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PATENT APPLICATION
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(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 3923US (99-0033)

First Inventor or Application Identifier Warren M. Farnworth

Title See 1 in Addendum

Express Mail Label No. EL500248887US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
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(preferred arrangement set forth below)

- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 4]

4. Oath or Declaration [Total Pages 2]

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- b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
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Signed statement attached deleting
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see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a
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- 9. ☒ 37 C.F.R. § 3.73(b) Statement ☒ Power of Attorney
(when there is an assignee)
- 10. ☐ English Translation Document (if applicable)
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- 12. ☐ Preliminary Amendment
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APPLICATION FOR LETTERS PATENT

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**STEREOLITHOGRAPHIC METHODS FOR FORMING A PROTECTIVE
LAYER ON A SEMICONDUCTOR DEVICE SUBSTRATE AND
SUBSTRATES INCLUDING PROTECTIVE LAYERS SO FORMED**

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**STEREOLITHOGRAPHIC METHODS FOR FORMING A PROTECTIVE
LAYER ON A SEMICONDUCTOR DEVICE SUBSTRATE AND
SUBSTRATES INCLUDING PROTECTIVE LAYERS SO FORMED**

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BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates generally to stereolithography and, more specifically, to the use of stereolithography to form protective layers on substrates, such as semiconductor dice or wafers, and the resulting structures.

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State of the Art: In the past decade, a manufacturing technique termed "stereolithography", also known as "layered manufacturing", has evolved to a degree where it is employed in many industries.

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Essentially, stereolithography as conventionally practiced, involves utilizing a computer to generate a three-dimensional (3-D) mathematical simulation or model of an object to be fabricated, such generation usually effected with 3-D computer-aided design (CAD) software. The model or simulation is mathematically separated or "sliced" into a large number of relatively thin, parallel, usually vertically superimposed layers, each layer having defined boundaries and other features associated with the model (and thus the actual object to be fabricated) at the level of that layer within the exterior boundaries of the object. A complete assembly or stack of all of the layers defines the entire object, and surface resolution of the object is, in part, dependent upon the thickness of the layers.

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The mathematical simulation or model is then employed to generate an actual object by building the object, layer by superimposed layer. A wide variety of approaches to stereolithography by different companies has resulted in techniques for fabrication of objects from both metallic and non-metallic materials. Regardless of the material employed to fabricate an object, stereolithographic techniques usually involve disposition of a layer of unconsolidated or unfixed material corresponding to each layer within the object boundaries, followed by selective consolidation or fixation of the material to at least a semi-solid state in those areas of a given layer corresponding to portions of the object, the consolidate or fixed material also at that time being substantially concurrently bonded to a lower layer. The unconsolidated material employed to build an object may be

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generally built in small quantities or where a product design is rendered only once. Finally, it has been appreciated in some industries that stereolithography provides a capability to fabricate products, such as those including closed interior chambers or convoluted passageways, which cannot be fabricated satisfactorily using conventional manufacturing techniques.

However, to the inventors' knowledge, stereolithography has yet to be applied to mass production of articles in volumes of thousands or millions, or employed to produce, augment or enhance products including other pre-existing components in large quantities, where minute component sizes are involved, and where extremely high resolution and a high degree of reproducibility of results is required.

In the electronics industry, computer chips are typically manufactured by configuring a large number of integrated circuits on a wafer, and subdividing the wafer to form singulated devices. A coating of protective dielectric material such as polyimide can be formed over the wafer prior to cutting, in order to prevent physical damage to each die and the circuitry thereon during handling of the die. Polyimide coatings are formed by applying a liquid polymer in a volatile carrier to the center of a spinning wafer. Thus, the polyimide layer is said to be "spun on" to the wafer. Typically, such polyimide layers have thicknesses of about 6μ . When the volatile carrier evaporates, as the polyimide layer shrinks, it warps, with the polyimide layer typically being thicker at the periphery of the wafer than at the center of the wafer, a phenomenon referred to as "dishing". Given the required tolerances for semiconductor devices, even slight dishing may drastically reduce the yield of useable dice from the wafer. Moreover, when polyimide layers are spun onto semiconductor wafers in this manner it is difficult to provide a repeatable thickness between wafer batches.

In addition, the cure temperature typically required to adequately cross-link the polyimide layer is typically about 300°C . This high cure temperature may be detrimental to the integrated circuits of the dice, as well as to the bond pads exposed at the active surface of the dice.

As conventional processes, such as spin-on techniques, form polyimide layers that substantially cover an active surface of a wafer, shrinkage or warpage of the polyimide layer during evaporation or volatilization of the carrier material or during curing can stress the wafer, and may damage the circuitry of semiconductor devices on the wafer.

Moreover, the resulting cure of the polyimide layer may not be a full "hard" cure. Consequently, if a die having such a polyimide layer on the active surface thereof is packaged with a polymer filled with particles of silica, such as sand with low α particle emission, the silica particles can impinge, or pass through, the polyimide layer, which is supposed to act as a physical barrier to the silica. Such impingement of silica particles can damage the circuits of the die, unless expensive round silica particles are used as a filler in the packaging material.

After disposal on the active surfaces of one or more dice and curing of the polyimide layer, each of the bond pads covered by the polyimide layer is exposed to facilitate access to the bond pads. Typically, a complex, conventional mask and etch process is employed. For example, a photoresist material may then be used to form a mask and an etchant can be employed to remove portions of the polyimide layer that overlies bond pads through apertures of the mask. As is well-known in the art, slight dimensional differences between wafers, including non-flatness, can occur, causing misalignment or distortion of the mask and, thus, of structures formed therethrough, such as the bond pad openings through a protective polyimide layer.

The use of a mask and etch processes to pattern polyimide protective layers is also somewhat undesirable in that these processes introduce additional fabrication steps and, thus, increase fabrication time, as well as increasing the likelihood that the die or dice being fabricated will be damaged. The use of mask and etch processing also consumes expensive dielectric materials and etchants.

Finally, as is well known to those in the art, alpha particles emitted by solders, leads, sand, and other sources can create electron-hole pairs in a semiconductor device and thereby cause "soft" errors during the operation of the semiconductor device. While not permanently damaging to the semiconductor device, "soft" errors are often a nuisance

to the user of a computer or other electronic device. A 6 μ layer of polyimide may act to minimize such "soft" errors.

The art does not teach methods of fabricating protective layers on the active surfaces of semiconductor devices that do not stress a wafer on which the semiconductor devices are contained or that do not require a significant number of additional fabrication steps. Nor does the art teach protective layers so fabricated that reduce the incidence of soft errors in the protected semiconductor devices.

SUMMARY OF THE INVENTION

The present invention provides a method of applying a layer of protective material to precisely defined areas on individual semiconductor devices fabricated on a semiconductor wafer, on individual dice, or on other semiconductor device component substrates. The present invention employs computer-controlled, 3-D computer-assisted drawing (CAD) initiated, stereolithographic techniques to rapidly form precision layers of material to specific surfaces of a substrate, such as a plurality of dice on a wafer, and to an individual die.

In a preferred embodiment, the layer and associated structures are fabricated on the substrate using precisely focused electromagnetic radiation in the form of an ultraviolet (UV) wavelength laser to fix or cure a liquid material in the form of a photopolymer. However, the invention is not so limited, and other stereolithographically-applicable materials may be employed in the present invention.

For example, a silicon wafer comprising a large number of distinct semiconductor devices may be covered with a layer of liquid polyimide or other photopolymer which is cured only in particular locations to an at least semisolid state by precisely directed laser radiation at a substantially ambient temperature. As the regions of the layer that are cured by the laser may be selected, photopolymer located over the contact pads of the substrate can be left uncured. Thus, apertures are formed through the protective layer substantially simultaneously with formation of the protective layer. A single layer having a uniform thickness of, for example, about 25 μ m (1 mil) may be formed on the surface of the wafer.

Single layers having thicknesses of up to about 10 mil or more may be formed, the maximum possible thickness of each layer being limited only by the maximum depth into the liquid photopolymer that the laser beam can penetrate. Multiple superimposed layers, each separately cured, may be formed to create a protective layer of even greater thickness while maintaining a thickness accuracy not achievable by conventional techniques. Multiple superimposed layers may also be used to form one or more three-dimensional structures on the surface of the protective layer or on the surface of the substrate.

When protective layers are being formed on a wafer bearing a plurality of semiconductor devices, the protective layer may have several laterally separated regions, each corresponding to the location of one of the semiconductor devices and having apertures formed therethrough to expose bond pads of the semiconductor devices. Further, "streets" traversing the wafer between adjacent semiconductor devices may also be left uncoated, thereby reducing stress to which the wafer would otherwise be exposed if a continuous, protective layer covered the semiconductor devices and the streets therebetween. Thus, for example, each semiconductor device on a wafer may be covered with a discrete, well-defined pattern of protective material of controlled depth, shape, and size, with precisely located apertures therethrough.

The robust, relatively thick protective layer formed in accordance with teachings of the present invention may be used to physically protect, seal, and isolate circuitry of semiconductor device components from physical damage that may occur during handling, as well as electrical shorting of a semiconductor device component to other devices, damage by chemical agents, and alpha particle-induced "soft" errors. When thermoplastic materials that soften or melt at temperatures that will not damage the semiconductor device are used as the protective layer, the protective layer can also act to adhere the semiconductor device to a higher level substrate. Such protective layers are particularly useful on a die to be packaged in a "leads over chip" (LOC)-type arrangement where, when packaged, the leads extend over and are secured to the active surface of the semiconductor die. The protective layer may also be applied following the attachment of leads to the bond pads of a semiconductor die, for example, around the lead fingers.

The apparatus used in the present invention may also incorporate a machine vision system to locate substrates, individual semiconductor devices on a wafer, and features on substrates.

The method of the present invention encompasses the use of all known stereolithography apparatus and the application of any and all materials thereby, including both metallic and non-metallic materials applied in any state and cured or otherwise fixed to at least a semi-solid state to define a layer or layers having identifiable boundaries.

Other features and advantages of the present invention will become apparent to those of skill in the art through a consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The drawings of the application illustrate exemplary embodiments of the invention, wherein the illustrated features are not necessarily to scale, wherein like indicia is used for like and similar elements, and wherein:

FIG. 1 is a schematic side elevation of an exemplary stereolithography apparatus suitable for use in practicing the method of the present invention;

FIG. 2 is an enlarged, schematic top view of a multiple-die wafer mounted on a platform for formation of a protective layer on the dice in accordance with the method of the invention;

FIG. 3 is a further enlarged top view of a portion of the wafer of FIG. 2 illustrating several configurations of a protective layer formed by the method of the invention;

FIG. 4 is a side cross-sectional view taken along line 4--4 of FIG. 3 and depicting a die of an exemplary wafer prior to formation of a protective layer thereon;

FIG. 5 is a side cross-sectional view taken along line 5--5 of FIG. 3 and depicting a die of an exemplary wafer having a protective layer thereon;

FIG. 6 is a side cross-sectional view taken along line 6--6 of FIG. 3 and depicting a die of an exemplary wafer having a protective layer thereon;

FIG. 7 is a side cross-sectional view taken along line 7--7 of FIG. 3 and depicting a die of an exemplary wafer having a protective layer thereon;

FIG. 8 is a side cross-sectional view taken along line 8--8 of FIG. 3 and depicting a die of an exemplary wafer having a protective layer thereon;

FIG. 9 is a side cross-sectional view taken along line 9--9 of FIG. 3 and depicting a die of an exemplary wafer having a protective layer thereon;

FIG. 10 is a side cross-sectional view of a lead frame-mounted die having a protective layer formed thereon in accordance with the invention; and

FIG. 11 is a side cross-sectional view of a lead frame-mounted die configured for forming a protective layer thereon in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 depicts schematically various components, and operation, of an exemplary stereolithography apparatus 10 to facilitate the reader's understanding of the technology employed in implementation of the present invention, although those of ordinary skill in the art will understand and appreciate that apparatus of other designs and manufacture may be employed in practicing the method of the present invention. The preferred stereolithography apparatus for implementation of the present invention as well as operation of such apparatus are described in great detail in United States Patents assigned to 3D Systems, Inc. of Valencia, California, such patents including, without limitation, U.S. Patents 4,575,330; 4,929,402; 4,996,010; 4,999,143; 5,015,424; 5,058,988; 5,059,021; 5,059,359; 5,071,337; 5,076,974; 5,096,530; 5,104,592; 5,123,734; 5,130,064; 5,133,987; 5,141,680; 5,143,663; 5,164,128; 5,174,931; 5,174,943; 5,182,055; 5,182,056; 5,182,715; 5,184,307; 5,192,469; 5,192,559; 5,209,878; 5,234,636; 5,236,637; 5,238,639; 5,248,456; 5,256,340; 5,258,146; 5,267,013; 5,273,691; 5,321,622; 5,344,298; 5,345,391; 5,358,673; 5,447,822; 5,481,470; 5,495,328; 5,501,824; 5,554,336; 5,556,590; 5,569,349; 5,569,431; 5,571,471; 5,573,722; 5,609,812; 5,609,813; 5,610,824; 5,630,981; 5,637,169; 5,651,934;

5,667,820; 5,672,312; 5,676,904; 5,688,464; 5,693,144; 5,695,707; 5,711,911;
5,776,409; 5,779,967; 5,814,265; 5,850,239; 5,854,748; 5,855,718; 5,855,836;
5,885,511; 5,897,825; 5,902,537; 5,902,538; 5,904,889; 5,943,235; and 5,945,058. The
disclosure of each of the foregoing patents is hereby incorporated herein by reference.

5 Improvements in the conventional stereolithographic apparatus, as described in
copending application serial number 09/259,143, filed February 26, 1999, and of even
assignment, relate to a so-called "machine vision" system in combination with suitable
programming of the computer controlling the stereolithographic process. This
improvement eliminates the need for accurate positioning or mechanical alignment of
10 workpieces to which material is stereolithographically applied. Alignment of the laser
beam or other fixing agent may be item specific (i.e. die specific) so that a large number of
distinct semiconductor devices, or dice 52, on a wafer 60, each die 52 defined by "streets"
44, may each be accurately coated with a protective layer 50 to the same or differing
specifications with regard to numbers of sub-layers 51, layer thickness 40, and boundaries
15 58 of areas of dice 52 to be covered by each layer 50 of at least semisolid photopolymer
material. Using a machine vision system, accuracy of the process is not dependent on the
fiduciary mark 62 (FIG. 3) on a wafer 60 but on the visual recognition of specific physical
characteristics of a die 52 or other substrate, whether die 52 is part of a large wafer, a
partial wafer, or singulated.

20 With reference to FIGS. 1-9 and as noted above, a 3-D computer-aided drafting
("CAD") drawing of an object such as a protective layer 50 to be fabricated in the form of
a data file is placed in the memory of a computer 12 controlling the operation of apparatus
10, if computer 12 is not a CAD computer in which the original object design is effected.
In other words, an object design may be effected in a first computer in an engineering or
25 research facility and the data files transferred via wide or local area network, tape, disc,
CD-ROM or otherwise as known in the art to computer 12 of apparatus 10 to fabricate
layer 50 or another object comprising one or more applied sub-layers 51. Each
sub-layer 51 is formed or consolidated by a pass of the laser beam 28 into a layer of

photo-curable material, or photopolymer. The term "active surface" is used herein to denote the actual surface as well as vertical projections thereof.

The data is preferably formatted in an STL type computer file, STL being a standardized format employed by a majority of manufacturers of stereolithography equipment. Fortunately, the format has been adopted for use in many solid-modeling CAD programs, so often translation from another internal geometric database format is unnecessary. In the particular case where the apparatus 10 is to be used for applying only a single layer 50 of uniform thickness, the program may be somewhat simplified.

Apparatus 10 also includes a reservoir 14 (which may comprise a removable reservoir interchangeable with others containing different materials) of liquid material 16 to be employed in applying the intended layer 50 of protective material to the dice 52 of a wafer 60 or to singulated dice. In a currently preferred embodiment, the liquid material 16 is a photo-curable polymer (hereinafter "photopolymer") responsive to light in the UV wavelength range. The surface level 18 of the liquid material 16 is automatically maintained at an extremely precise, constant magnitude by devices known in the art responsive to output of sensors within apparatus 10 and preferably under control of computer 12. A support platform or elevator 20, precisely vertically movable in fine, repeatable increments in directions 46 responsive to control of computer 12, is located for movement downward into and upward out of liquid material 16 in reservoir 14. A UV wavelength range laser plus associated optics and galvanometers (collectively identified as 22) for controlling the scan of laser beam 26 in the X-Y plane across platform 20 has associated therewith mirror 24 to reflect beam 26 downwardly as beam 28 toward surface 30 of platform 20, or more particularly toward surface 54 of a wafer 60 positioned on surface 30. Beam 28 is traversed in a selected pattern in the X-Y plane, that is to say in a plane parallel to surface 30, by initiation of the galvanometers under control of computer 12 to at least partially cure, by impingement thereon, selected portions of liquid material 16 disposed over surface 54 to at least a semi-solid state. The use of mirror 24 lengthens the path of the laser beam 26, effectively doubling same, and provides a more vertical beam 28 than would be possible if the laser 22 itself were mounted directly above

platform surface 30, thus enhancing resolution. In the exemplary method described herein, a wafer 60 may be precisely coated with a protective layer irrespective of wafer size or number of dice 52. Thus, current stereolithographic equipment will accommodate wafers 60 up to 12 or more inches in X and Y dimensions, and it is expected that equipment size will increase as the ability to produce even larger wafers becomes commonplace. Base supports, not shown, may be placed on platform 20 prior to introduction of the wafer 60, to support the wafer 60 in a highly planar, level position. Apparatus 10 may be programmed to stereolithographically form such supports on platform 20.

While the invention is described in terms of a liquid material polymerizable to a semi-solid and/or solid, the process may be varied to use a powdered material, for example. The term "unconsolidated" will be used herein to denote the unpolymerized material, which becomes "altered" or "consolidated" by the laser radiation to at least a semi-solid state.

Wafer 60 or another substrate may be secured to the platform 20 so that it will not move thereon during formation of the layer 50. As seen in FIGS. 2 and 4, wafer 60 may be attached to the platform 20 by at least two small edge supports 38, which may be formed in situ by apparatus 10 prior to forming layers 50 on the dice 52 of the wafer 60. Edge supports 38 are formed from liquid photopolymer material 16 which is at least partially cured by a laser beam 28 prior to forming layers 50 on the dice 52. The locations of edge supports 38 are preferably at the edges 42 of unusable partial dice 52A (on a round wafer 60), and align the wafer edge 42 and to surface 30 of the platform 20. Edge supports 38 may be formed prior to placing a wafer 60 on platform 20 and configured to hold wafer 60 in place upon platform 20. Edge supports 38 may also be configured to align wafer 60 on platform 20. Alternatively, edge supports 38 may be formed after a wafer 60 has been positioned on platform. Edge supports 38 may be formed of a partially cured material whose attachment to the platform is readily releasable, or a solvent may be used to dissolve the edge supports 38. Such solvent materials are known in the art. See, for example, U.S. Patent No. 5,447,822 referenced above and previously incorporated

herein by reference. The data for forming such edge supports 38 may be programmed as a separate STL file.

A camera 70 is then activated to locate the position and orientation of each die 52 or other substrate on which a layer 50 is to be placed by scanning platform 20 and comparing the features of dice 52 with those in the data file residing in memory, the locational and orientational data for each die then also being stored in memory. It should be noted that the data file representing the design size, shape, and topography for dice 52 or other substrates may be used at this juncture to detect physically defective or damaged dice 52. It should also be noted that data files for more than one type (size, thickness, configuration, surface topography) of a die 52 or other substrate may be placed in computer memory and computer 12 programmed to recognize locations and orientations of dice 52 or other substrates, as well as the boundaries 58 which define the layer 50 which is to be formed, and a laser path for forming the layer.

Referring now to both FIGs. 1 and 2, data from the STL files resident in computer 12 is manipulated to form layer 50 one sub-layer 51 at a time on each die 52 or other substrate. Accordingly, where layer 50 is formed of a plurality of individually formed sub-layers 51, the data mathematically representing layer 50 is divided into subsets, each subset representing a slice or sub-layer 51 of layer 50. This is effected by mathematically sectioning the 3-D CAD model into a plurality of horizontal sub-layers 51, a "stack" of such sub-layers 51 representing layer 50. Each slice or sub-layer 51 may be from about 0.0001 to about 0.0300 inch thick. As mentioned previously, a thinner slice promotes higher resolution by enabling better reproduction of fine vertical surface features of sub-layer 51. Where a "recoater" blade 32 is employed as described below, the interposition of base supports precludes inadvertent contact of blade 32 with the surface 54 of wafer 60 or the surface of another substrate.

Before fabrication of layer 50 is initiated with apparatus 10, the primary STL file is configured for the particular dice 52 or other substrates upon which layers 50 are to be formed. Thus, by way of example and not by way of limitation, the primary STL file is integrated with the file used for forming the integrated circuits on the dice 52 or the

features on other substrates. It should be recognized that, while reference is made herein to sequentially forming a layer 50 on dice 52 of a wafer 60, the same process may be used to form a layer on a singulated die 52 or other individual substrate. Furthermore, a wafer 60 having dice 52 of differing dimensions and/or layout may be accommodated by merging of the STL files of the different dice 52 into the primary STL file. Operational parameters for apparatus 10 are then set, for example, to adjust the size (e.g., diameter, if circular) of the laser light beam 28 used to alter the state of, i.e., cure material 16.

Before initiation of a first sub-layer 51 of layer 50 is commenced, computer 12 automatically checks and, if necessary, adjusts by means known in the art, the surface level 18 of liquid material 16 in reservoir 14 to maintain same at an appropriate focal length for laser beam 28. U.S. Patent 5,174,931, referenced above and previously incorporated herein by reference, discloses one suitable level control system. Alternatively, the height of mirror 24 may be adjusted responsive to a detected surface level 18 to cause the focal point of laser beam 28 to be located precisely at the surface of liquid material 16 at surface level 18 if level 18 is permitted to vary, although this approach is somewhat more complex. The platform 20 may then be submerged in liquid material 16 in reservoir 14 to a depth equal to the thickness of one sub-layer 51 or slice of the layer 50 or another object to be fabricated, and the liquid surface level 18 readjusted as required to accommodate liquid material 16 displaced by submergence of platform 20. Laser 22 is then activated so that laser beam 28 will scan liquid material 16 in a defined path over surface 54 of each substrate, such as the illustrated die 52, in turn to at least partially cure (e.g., at least partially polymerize) liquid material 16 at selective locations on each die 52. For example, laser 22 first defines the boundaries 58 of a first sub-layer 51 on die 52 and fills in solid portions thereof to complete the layer. The boundaries 58 may circumscribe bond pads 34 or other features on die surface 56 of die 52 which are intended to be left exposed for connection to higher-level packaging as by wire bonding, tape-automated bonding ("TAB") using flex circuits, use of projecting conductive connectors in a "flip-chip" configuration, or otherwise, as known in the art. The circumscription of such features is specified in the STL files in computer 12. In the event that complete layer 50

comprises more than one single sub-layer 51, platform 20 is then lowered by a distance equal to thickness of a layer 51, and the laser beam 28 scanned to define and fill in a second sub-layer 51 while simultaneously bonding the second sub-layer 51 to the first sub-layer 51. The process is then repeated, sub-layer by sub-layer, until layer 50 is completed.

If a recoater blade 32 is employed, the process sequence is somewhat different. In this instance, the surface 30 of platform 20 is lowered into liquid material 16 below surface level 18, then raised thereabove until it is precisely a thickness 36 of sub-layer 51 below blade 32. Blade 32 then sweeps horizontally over surface 56 of die 52, or (to save time) at least over a portion thereof on which layer 50 is to be fabricated, to remove excess liquid material 16 and leave a film thereof of the precise, desired thickness on surface 56. Platform 20 is then lowered so that the surface of the film and material level 18 are coplanar and the surface of the material 16 is still. Laser 22 is then initiated to scan with laser beam 28 and define the first sub-layer 51. The process is repeated, sub-layer by sub-layer, to define each succeeding sub-layer 51 and simultaneously bond same to the next lower sub-layer 51 until layer 50 is completed. The process is then repeated for each die 52 of wafer 60 or on each of another type of semiconductor device component substrate on which a layer 50 is to be formed. A more detailed discussion of this sequence and apparatus for performing same is disclosed in U.S. Patent 5,174,931, previously incorporated herein by reference.

As an alternative to the above approach to preparing a layer of liquid material 16 for scanning with laser beam 28, a layer of liquid material 16 may be formed on surface 56 of a substrate, such as the illustrated die 52, by lowering platform 20 to flood material over surface 56 or over the highest completed sub-layer 51 of layer 50, then raising platform 20 and horizontally traversing a so-called "meniscus" blade across the platform (or just the formed portion of layer 50) of a thickness equal to one sub-layer 51 thereabove, followed by initiation of laser 22 and scanning of beam 28 to define the next higher sub-layer 51.

As yet another alternative to layer preparation of liquid material 16 is to merely lower platform 20 to a depth equal to that of a layer of liquid material 16 to be scanned and then traverse a combination flood bar and meniscus bar assembly horizontally over platform 20 to substantially concurrently flood liquid material 16 over surface 54 of wafer 60 and define a precise layer thickness of liquid material 16 for scanning.

All of the foregoing approaches to flooding and layer definition and apparatus of initiation thereof are known in the art, and so no further details relating thereto will be provided.

Each sub-layer 51 of complete layer 50 is preferably built by first defining any internal and external object boundaries 58 of that sub-layer 51 with laser beam 28, then hatching solid areas of complete layer 50 with laser beam 28. If a particular part of a particular sub-layer 51 is to form a boundary 58 of a void in the object above or below that sub-layer 51, then the laser beam 28 is scanned in a series of closely-spaced, parallel vectors so as to develop a continuous surface, or skin, with improved strength and resolution. The time it takes to form each sub-layer 51 depends upon its geometry, surface tension and viscosity of material 16, and thickness of the layer.

Once the layers 50 or other objects are completed on the substrate, such as the illustrated dice 52 of wafer 60, platform 20 is elevated above surface level 18 of liquid material 16, and wafer 60 with protective layers 50 on dice 52 thereof may be removed from apparatus 10. Excess, uncured liquid material 16 on the surface of wafer 60 may be removed, for example by a manual removal step and solvent-cleaning. Layer 50 on each die 52 of wafer 60 may then require postcuring, as material 16 may be only partially polymerized and exhibit only a portion (typically 40% to 60%) of its fully cured strength. Postcuring to completely harden layers 50 over the entire wafer 60 or portions thereof, on singulated dice 52, or on other semiconductor device component substrates may be effected in another apparatus projecting UV radiation in a continuous manner over wafer 60 or dice 52 and/or by thermal completion of the initial, UV-initiated partial cure. Singulation of the individual dice 52 of a wafer 60 is preferably done following the completed cure, but may also be effected prior to a completed cure.

A small portion of wafer 60 is shown in FIG. 3, having a plurality of rectangular dice 52, 52B, 52C, 52D, 52E and 52F, etc. with die edges 48 separated by streets 44 in the X and Y directions. FIGS. 3 and 4 illustrate a die 52B with bond pads 34 at an edge thereof, prior to the formation of a protective layer 50 on die 52. For the sake of simplicity, other details of the surface 56 of die 52 are not shown.

FIGS. 3 and 5 illustrate the same type of die 52B with a sub-layer 51 of protective material formed thereon within boundary 58. Boundary 58 excludes the entire end of the die 52B having bond pads 34 thereon.

In FIGS. 3 and 6, die 52C has two rows of centrally located bond pads 34. Coverage by sub-layer 51 is complete except for the bond pads 34 and adjacent areas.

As shown in FIGS. 3 and 8, die 52E has a first sub-layer 51 on the surface thereof. A second sub-layer 51A is then formed over particular areas of layer 51 to increase the thickness of layer 50 in those areas. Again, the bond pads 34 and adjacent areas are exempted from coverage by both sub-layers 51, 51A. It is noted that in this method, the walls of apertures formed through layer 50 above a bond pad 34 may be substantially vertical, angled or otherwise shaped. When layer 50 has a plurality of sub-layers, the orientation or configuration of the aperture walls can be programmed into the STL file.

The ability to precisely direct the laser beam 28 to uniformly cover a small target area enables the method to provide very accurate and precise inner or outer boundaries 58. As illustrated in FIGS. 3 and 9, die 52F is shown with a sub-layer 51 precisely surrounding each bond pad 34. Similarly, in FIGS. 3 and 7, die 52D is illustrated as representing a die surface 56 covered by protective sub-layer 51. Sub-layer 51 is formed so as to leave bond pads 34, which are located in centrally extending rows, exposed therethrough.

The various types of layer coverage depicted in FIGS. 3-9 are exemplary only and not intended to be limiting. Any portion of any die 52 of any configuration may have a layer 50 formed thereon by this invention, using one material layer or two or more superimposed, contiguous, mutually-adhered sub-layers 51.

When layer 50 or regions thereof are fabricated from a thermoplastic material having a softening or melting temperature that is will not damage die 52, the thermoplastic regions of layer 50 may also be used as an adhesive, or glue, to secure die 52 to a substrate in face-down orientation. The thermoplastic material of layer 50 is disposed in a configuration and thickness that, when heated to at least the softening temperature thereof, will adhere die 52 to a substrate or other component of a semiconductor device assembly in a desired manner. When the material of layer 50 softens at a temperature that also wets or melts conductive structures secured to bond pads 34 while continuing to laterally support the conductive structures, die 52 may be secured to a substrate or other component of a semiconductor device assembly substantially simultaneously with the electrical connection of a conductive structure to a contact of the other component.

In practicing the present invention, a commercially available stereolithography apparatus operating generally in the manner as that described with respect to apparatus 10 of FIG. 1 is preferably employed. For example and not by way of limitation, the SLA-250/50HR, SLA-5000 and SLA-7000 stereolithography systems, each offered by 3D Systems, Inc, of Valencia, California are suitable for practice of the present invention. Photopolymers believed to be suitable for use in practicing the present invention include Cibatool SL 5170 and SL 5210 resins for the SLA-250/50HR system, Cibatool SL 5530 resin for the SLA-5000 and Cibatool SL 7510 resin for the SLA-7000 system. All of these resins are available from Ciba Specialty Chemicals Corporation. Materials are selected for dielectric constant, purity (semiconductor grade), good adherence to other semiconductor device materials, and a coefficient of thermal expansion (CTE) sufficiently similar to that of the dice 52 to which the material is applied so that the dice 52 and cured material thereon are not unduly stressed during thermal cycling in testing and subsequent normal operation. One area of particualr concern in determining resin suitability is the substantial absence of mobile ions and, specifically, fluorides. By way of example and not limitation, the layer thickness 40 of material 16 to be formed, for purposes of the invention, may be on the order of about 0.001 inch (1 mil) to about 0.020 inch (20 mils), with a high degree of uniformity over a field on a surface 56 of a die 52 or other substrate. In order to

achieve a desired physical, environmental, and alpha particle protection of a semiconductor die 52, it is presently believed that a preferred total layer thickness 40 is about 0.004 to about 0.015 inches (4 to 15 mils). As noted previously herein, such thicknesses may be achieved with a single layer. It should be noted that different sub-layers 51 may be of different thicknesses, so as to form a completed layer 50 of a precise, intended total height or to provide different material thicknesses for different portions of layer 50. The size of the laser beam "spot" impinging on the surface of liquid material 16 to cure same may be on the order of 0.002 inch to 0.008 inch. Resolution is preferably ± 0.0003 inch in the X-Y plane (parallel to platform surface 30) over at least a 0.5 inch X .25 inch field from a center point, permitting a high resolution scan effectively across a 1.0 inch X 0.5 inch area. Of course, it is desirable to have substantially this high a resolution across the entirety of surface 54 of a whole wafer 60 to be scanned by laser beam 28, such area being termed the "field of exposure". The longer and more effectively vertical the path of laser beam 26/28, the greater the achievable resolution.

Referring again to FIG. 1 of the drawings, improved performance of this process is achieved by certain additions to apparatus 10. As depicted, apparatus 10 includes a camera 70 which is in communication with computer 12 and preferably located, as shown, in close proximity to mirror 24 located above surface 54 of wafer 60 or another substrate on which a layer 50 according to the invention is to be formed. Camera 70 may be any one of a number of commercially available cameras, such as capacitive-coupled discharge (CCD) cameras available from a number of vendors. Suitable circuitry as required for adapting the output of camera 70 for use by computer 12 may be incorporated in a board 72 installed in computer 12, which is programmed as known in the art to respond to images generated by camera 70 and processed by board 72. Camera 70 and board 72 may together comprise a so-called "machine vision system", and specifically a "pattern recognition system" (PRS), operation of which will be described briefly below for a better understanding of the present invention. Alternatively, a self-contained machine vision system available from a commercial vendor of such equipment may be employed. For example, and without limitation, such systems are available from Cognex

Corporation of Natick, Massachusetts. The apparatus of the exemplary Cognex BGA Inspection Package™ or SMD Placement Guidance Package™ may be adapted to the present invention, although it is believed that the MVS-8000™ product family and the Checkpoint® product line, the latter employed in combination with Cognex PatMax™ software, may be especially suitable for use in the present invention.

It is noted that a variety of machine vision systems are in existence, examples of which and their various structures and uses are described, without limitation, in U.S. Patents 4,526,646; 4,543,659; 4,736,437; 4,899,921; 5,059,559; 5,113,565; 5,145,099; 5,238,174; 5,463,227; 5,288,698; 5,471,310; 5,506,684; 5,516,023; 5,516,026; and 5,644,245. The disclosure of each of the immediately foregoing patents is hereby incorporated by this reference.

In order to facilitate practice of the present invention with apparatus 10, a data file representative of the surface of a substrate, such as a die 52 or wafer 60, on which a layer 50 is to be formed is placed in the memory of computer 12. The data file will contain information such as, for example, die surface dimensions and visual features of the substrate. When the substrate is a wafer, the data file can also include information about the spacing and layout of dice 52 on wafer 60. The data file will also contain information defining the specific area(s) of the surface of the substrate which are to be covered with layer 50 and the desired depth of coverage, and in addition, a defined path of laser beam 28 as controlled by mirror 24 to achieve the desired coverage.

Continuing with reference to FIG. 1 of the drawings, a substrate, such as the illustrated wafer 60, on platform 20 may be submerged partially below the surface level 18 of liquid material 16 to a depth the same as, or greater than, the desired thickness 40 of a first sub-layer 51 of material 16 to be at least partially cured to a semisolid state, and then raised to a depth equal to the layer thickness 40 if lowered to a greater depth than a layer thickness, the surface level 18 of liquid material 16 being allowed to stabilize. The material 16 selected for use in applying a protective layer 50 to dice 52 may be one of the above-referenced resins from Ciba Specialty Chemical Company which exhibits a desirable dielectric constant, is of sufficient (semiconductor grade) purity, of a desirable hardness

for physical protection, and which is similar in coefficient of thermal expansion (CTE) to that of the substrate, such as die 52, on which layer 50 is to be formed so that neither the substrate nor layer 50 are unduly stressed during thermal cycling in subsequent packaging, testing and normal operation.

5 Laser 22 is then activated and scanned to direct beam 28, under control of computer 12, across the desired portion of the surface of the substrate (e.g., surface 56) to effect the partial cure of material 16 to form a first sub-layer 51 on the substrate. If the substrate is a die 52 or a wafer 60, the laser 22 is then refocused to another die 52 and the process repeated. If any portion of die surface 56 is to have a second (or more)
10 sub-layer(s) 51, the platform 20 is lowered further into reservoir 14, and can also be raised as before, to submerge the substrate and formed sub-layers 51 into liquid material 16. The laser is then activated to form another sub-layer 51A atop sub-layer 51, for example. It should be noted that thickness 40 of material 16 over a selected portion of a given substrate (e.g., die 52) may be altered die by die, again responsive to output of camera 70
15 or one or more additional cameras 74, 76, and 78, shown in broken lines, which detect particular features of the substrate.

It should be noted that the laser treatment may be carried out to form a boundary 58 which adheres to the surface (e.g., die surface 56) of the substrate and the sub-layer 51 within the boundary is lightly cured to form a semi-solid "skin" which
20 encloses liquid material 16. Trapped, unconsolidated material will eventually cure due to the cross-linking initiated in the outwardly adjacent photopolymer. The cure of sub-layer 51 may be subsequently accelerated by broad-source UV radiation in a chamber, or by thermal cure in an oven. In this manner, an extremely thick protective layer 50 may be formed in minimal time within apparatus 10.

25 As illustrated in FIG. 10, the method of the invention may be adapted to form layers 50 on dice 52 (e.g. LOC dice) already mounted on lead frames 66. In the example of FIG. 10, a series of dice 52 have active surfaces 64 secured to lead frames 66 of strip 80 and electrically connected thereto, such as by wire bonding, thermocompression bonding, TAB bonding, or otherwise as known in the art. A layer 50 of semi-solid

material formed from material 16 may be formed on any particular portion of the active surface 64 or backside 82 (including lead frame 66) of each die 52, for protection, insulation or other purpose. In the example of FIG. 10, a layer 50 of semi-solid material is to be formed on portions of the active surface 64 of a die 52 suspended from lead frame strip 80 and supported on platform 20. Layer 50 surrounds lead fingers of the lead frame 66 and provides attachment thereof to die 52. As already described, a film of liquid material 16 is formed atop the active surface 64 and lead frame 66, and a narrow beam 28 of UV laser radiation is precisely scanned by stereolithographic means over particular areas to partially cure the material 16 to form a semi-solid layer 50. The lead frame strip 80 is then repositioned to place the next sequential die 52 in place for formation of layer 50. It should be noted that the process may be conducted without an underlying platform 20 provided that the die 52 and lead frame strip 80 are securely joined, and a vertical position of the combination may be precisely attained and retained without underlying support.

In another variation, shown in the example of FIG. 11, a narrow sub-layer 51 defining an attachment 84 of semi-solid material may be first formed with the dice 52 positioned atop the lead frame strip 80, this layer formed adjacent the periphery of the dice 52 to join outer portions of the lead fingers to the dice. Attachment 84 may be formed by submerging the lead frame strip and die to a level providing the desired reinforcement member and partially curing by laser radiation. Following this step, the lead frame strip 80 may then be inverted and a layer 50 applied to the active surface/lead frame side of the die 52, as indicated above.

It is notable that the method depicted and described with respect to FIGS. 10 and 11 have utility with a variety of lead frame configurations, including conventional lead frames having a die mounting paddle, or paddle-less leads-over-chip (LOC) lead frames or leads-under-chip (LUC) lead frames. The method is adaptable to dice 52 configured for packaging as zig-zag in-line (ZIP) packages, single in-line (SIP) packages, dual in-line packages (DIP), thin small outline packages (TSOP), quad flat packs (QFP), direct die connect packages (DDC), or otherwise.

It is also notable that the present invention provides a rapid method for forming layers of protective material precisely on specified areas of singulated dice 52, many dice of a wafer 60, or dice joined to a lead frame strip 80. The method conserves material 16, since all such material in which cure is not initiated by laser 28 remains in a liquid state in reservoir 14 for continued use.

As the packaging method of the present invention is conducted at substantially ambient temperature, the small beam spot size and rapid traverse of laser beam 28 on the semiconductor dice 52 or other substrate results in negligible thermal stress thereon.

Referring to FIGS. 1 through 10 of the drawings, it will be apparent to the reader that the present invention involves a substantial departure from prior applications of stereolithography, in that the structures of preformed electrical components are modified by forming layered structures thereon using computer-controlled stereolithography.

It should be re-emphasized that the stereolithographic technique of the present invention is suitable for covering, or leaving uncovered, any desired portion of a semiconductor device component substrate, such as semiconductor die 52, so that electrical connections for connection to lead frames, test equipment or higher-level packaging may be left bare.

While the present invention has been disclosed in terms of certain preferred embodiments, those of ordinary skill in the art will recognize and appreciate that the invention is not so limited. Additions, deletions and modifications to the disclosed embodiments may be effected without departing from the scope of the invention as claimed herein. Similarly, features from one embodiment may be combined with those of another while remaining within the scope of the invention.

CLAIMS

What is claimed is:

1. A method of fabricating a protective layer on a semiconductor device, comprising:
5 providing at least one semiconductor die having an active surface with at least one bond pad exposed thereover;
selecting at least one portion of said active surface to be covered with at least a first layer of a protective material;
forming said at least a first layer with said protective material in an unconsolidated state at
10 least over at least one portion; and
selectively altering the state of the first layer of protective material over at least a portion of said at least one portion from said unconsolidated state to at least a semisolid state, while leaving protective material over other portions of said active surface in said unconsolidated state.

2. The method of claim 1, wherein said forming said at least a first layer of said protective material in said unconsolidated state comprises forming said at least a first layer with said protective material being in a liquid state.

3. The method of claim 1, wherein said forming said at least a first layer comprises forming said at least a first layer of protective material in said unconsolidated state to have a thickness substantially the same as a desired thickness of said protective material in said at least semisolid state over said at least one portion.

4. The method of claim 1, wherein said selectively altering comprises directing a controlled, discrete beam of radiation onto said protective material located over said at least one portion.

5. The method of claim 4, wherein said directing comprises directing a controlled, discrete beam of focused ultraviolet laser radiation.

6. The method of claim 1, wherein said forming said at least a comprises forming said at least a from a liquid resin controllably curable to a solid state.

7. The method of claim 1, wherein said providing comprises providing a wafer having a plurality of semiconductor dice.

8. The method of claim 1, further comprising:
selecting at least one second portion of said active surface covered with said at least a first layer of protective material to be covered with a second layer of protective material, said at least one second portion being superimposed, contiguous with, and mutually adhered to said at least one portion of said at least a first layer;
forming said second layer with said protective material in an unconsolidated state over at least said at least one second portion of said active surface; and
selectively altering the state of said second layer of material over at least a portion of said at least one second portion from said unconsolidated state to at least a semisolid state while leaving protective material of said second layer over other regions of said active surface in said unconsolidated state.

9. The method of claim 1, further comprising removing at least some of said protective material in said unconsolidated state from said at least one semiconductor die.

10. The method of claim 9, further comprising subjecting said semisolid protective material over at least one semiconductor die to a substantially full cure.

11. The method of claim 1, wherein said selectively altering comprises leaving protective material over said at least one bond pad in said unconsolidated state.

12. A method of forming a layer of protective material on a specified area on an active surface of one or more selected dice of a plurality of semiconductor dice of a wafer, comprising:

5 selecting at least one portion of said active surface of each of the selected dice to be covered with the layer of protective material;
forming a at least a of protective material in an unconsolidated state over at least said at least one portion of the active surfaces;
selectively altering the state of said protective material of said at least a over at least at portion of said at least one portion of the active surfaces to at least a semisolid state, while leaving the protective material over other regions of the active surfaces
10 in a substantially unconsolidated state.

13. The method of claim 12, further comprising:
selecting at least one second portion of said active surface at least partially overlying said
15 at least one portion of said at least a to be covered with a second layer of protective material;
forming said second layer with said protective material in an unconsolidated state over at least one second portion; and
selectively altering the state of the protective material of said second layer over at least a
20 portion of said at least one second portion from said unconsolidated state to an at least semisolid state, said at least one second portion being superimposed over, contiguous with, and mutually adhered to said at least one portion of said at least a, while leaving protective material of said second layer over other regions of the active surfaces in said unconsolidated state.

14. The method of claim 12, further comprising removing at least some of the protective material in said unconsolidated state from said active surfaces.

15. The method of claim 13, further comprising subjecting at least the protective material in said at least semisolid state to a secondary curing for further solidifying the protective material.

5 16. The method of claim 12, further comprising singulating at least the selected dice from the wafer.

17. The method of claim 16, further comprising singulating at least the selected dice from the wafer.

10 18. The method of claim 18, wherein said singulating is effected before said secondary curing.

15 19. The method of claim 18, wherein said singulating is effected after said secondary curing.

20 20. The method of claim 12, wherein said selectively altering comprises leaving the protective material overlying regions of the wafer lying between adjacent ones of the selected dice in said unconsolidated state.

21. The method of claim 12, wherein said forming said at least a comprises substantially completely covering the wafer with the protective material in said unconsolidated state.

25 22. The method of claim 12, wherein said selectively altering comprises leaving protective material over bond pads of the selected dice in said unconsolidated state.

23. The method of claim 12, wherein said selectively altering comprises subjecting said at least said portion of said at least one portion to a beam of radiation.

24. A method for forming a protective layer on a selected portion of a surface of a semiconductor die, comprising:
providing the semiconductor die with an active surface thereof being attached to a lead frame of a lead frame strip;
5 supporting the semiconductor die on a platform with a backside of the semiconductor die being placed on said platform;
submerging at least the semiconductor die in liquid resin to form a layer of said liquid resin over said active surface;
subjecting said selected portions of said layer to a controllable beam of radiation to change
10 said liquid resin in said selected portions to an at least semisolid state.

25. The method of claim 24, wherein said subjecting comprises subjecting said selected portions a beam of UV radiation.

26. The method of claim 24, further comprising storing data including at least one physical parameter of the semiconductor die in computer memory, and using the stored data in conjunction with a machine vision system to recognize the location and orientation of the semiconductor die and said selected portion.

27. The method of claim 26, further comprising using the stored data, in conjunction with the machine vision system, to selectively form said layer of material stereolithographically over said selected portion of said die.

28. The method of claim 24, wherein said subjecting comprises subjecting portions of said layer other than at locations of leads of the lead frame.

29. The method of claim 24, wherein said forming comprises forming said layer with at least a portion thereof underlying a lead of the lead frame.

30. The method of claim 29, further comprising removing at least some of said protective material in said unconsolidated state from said active surface.

31. The method of claim 30, further comprising subjecting at least said protective material in said unconsolidated state to a secondary curing.

32. The method of claim 31, wherein said secondary curing comprises increasing a temperature of said protective material.

33. A method for forming a protective layer on a selected portion of the active surface of semiconductor dice of a wafer, comprising:
securing the wafer to a platform;
recognizing a location and orientation of at least one selected die of the wafer and bond pads on an active surface of said at least one selected die;
submerging said platform in a liquid resin to a controlled liquid depth at least over at least a portion of said active surface of said at least one selected die; and
subjecting at least one selected portion of said liquid resin over said active surface of said at least one selected die to a discrete beam of focused radiation to alter said liquid resin in said at least one selected portion to at least a semisolid state and form a layer of semisolid material adhered to said active surface.

34. The method of claim 33, further comprising storing data including at least one physical parameter of said at least one selected die of the wafer, in computer memory, and using the stored data in cooperation with a machine vision system to recognize the location and orientation of said at least one selected die, and to control said path of said narrow beam of radiation to stereolithographically form said layer of semisolid material.

35. The method of claim 34, wherein said step of storing data comprises merging physical parameter data for said at least one selected die with data for controlling said subjecting.

5 36. The method of claim 33, wherein said securing the wafer to said platform comprises stereolithographically forming wafer supports on said platform to horizontally secure the wafer.

10 37. The method of claim 33, wherein said securing the wafer to said platform comprises placing said wafer on said platform and stereolithographically forming semisolid edge supports securing an edge of the wafer to said platform.

15 38. A semiconductor wafer having a plurality of dice, each die having a protective layer on selected portions thereof, said protective layer on one of said plurality of dice being substantially discontinuous from protective layers on adjacent ones of said plurality of dice.

20 39. The semiconductor wafer of claim 38, wherein each of said plurality of dice has conductors, said conductors of at least selected ones of said dice being exposed through said protective layer.

40. The semiconductor wafer of claim 39, wherein said conductors comprise bond pads.

25 41. The semiconductor wafer of claim 38, wherein said at least a portion of protective layer comprises a thermoplastic material.

42. The semiconductor wafer of claim 41, wherein said thermoplastic material comprises an adhesive.

43. A semiconductor device component having a layer of protective material on an active surface thereof, comprising:
a substrate with at least one conductor on the active surface thereof; and
a plurality of layers of at least semisolid photopolymer material on the active surface, said
5 plurality of layers being of superimposed, contiguous, and mutually adhered, each
layer of said plurality of layers being substantially free of voids and air pockets,
said at least one conductor being electrically exposed through said plurality of
layers.

10 44. The semiconductor device component of claim 43, wherein said at least
one conductor is laterally surrounded by said at least semisolid photopolymer material of
at least some layers of said plurality of layers.

15 45. The semiconductor device component of claim 43, wherein a surface of
said plurality of layers is planar.

46. The semiconductor device component of claim 43, wherein a surface of
said plurality of layers is substantially parallel to the active surface.

20 47. The semiconductor device component of claim 43, wherein said substrate
comprises a semiconductor die.

48. The semiconductor device component of claim 43, wherein said substrate
comprises a wafer with a plurality of dice.

25 49. The semiconductor device component of claim 48, wherein said plurality of
layers each exhibit a discontinuous region located over streets of said wafer between
adjacent dice.

50. The semiconductor device component of claim 43, wherein at least an outermost of said plurality of layers comprises an adhesive material.

51. The semiconductor device component of claim 50, wherein said adhesive material comprises thermoplastic material.

52. A method for securing a component of a semiconductor device assembly to another component of the semiconductor device assembly, comprising:
providing the component, the component including a plurality of superimposed,
contiguous, mutually adhered layers of material on a surface thereof, at least an
outermost of said layers comprising an adhesive material;
aligning the component with the another component;
securing the component to the another component with said adhesive material.

53. The method of claim 52, wherein said providing comprises providing the component with at least said outermost of said layers comprising a thermoplastic material.

54. The method of claim 53, wherein said securing comprises heating at least portions of said thermoplastic material to at least soften said thermoplastic material.

55. The method of claim 54, further comprising, substantially simultaneously with said heating at least portions of thermoplastic material, heating at least one conductive structure of at least one of the component and the another component to secure said at least one conductive structure to a contact of the other of the component and the another component.

56. The method of claim 52, further comprising securing at least one conductive structure of at least one of the component and the another component to a contact of the other of the component and the another component.

ABSTRACT OF THE DISCLOSURE

A stereolithographic method of applying material to form a protective layer on a preformed semiconductor die with a high degree of precision, either in the wafer stage, when attached to a lead frame, or to a singulated, bare die. The method is computerized and may utilize a machine vision feature to provide precise die-specific alignment. A semiconductor die may be provided with a protective structure in the form of at least one layer or segment of dielectric material having a controlled thickness or depth and a very precise boundary. The layer or segment may include precisely sized, shaped and located apertures through which conductive terminals, such as bond pads, on the surface of the die may be accessed. Dielectric material may also be employed as a structure to mechanically reinforce the die-to-lead frame attachment.

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A schematic diagram of a measurement system 10. A container 14 is shown with a base 16 and a vertical wall 18. A horizontal plate 20 is positioned inside the container. A laser source 22 is located outside the container, emitting a laser beam 26. The beam 26 passes through a lens or aperture 76 and is reflected by a mirror 24. The reflected beam 28 is directed downwards, passing through a lens or aperture 78, and is focused onto a target 30 on the plate 20. A sensor 32 is positioned to detect the reflected beam 28. A control unit 12 is connected to the laser source 22 and the sensor 32. A power supply 72 is connected to the control unit 12. A vertical scale 46 is shown on the right side of the container, with a horizontal line 54 indicating a measurement point. A dashed line 74 indicates the path of the laser beam 26.

FIG. 11

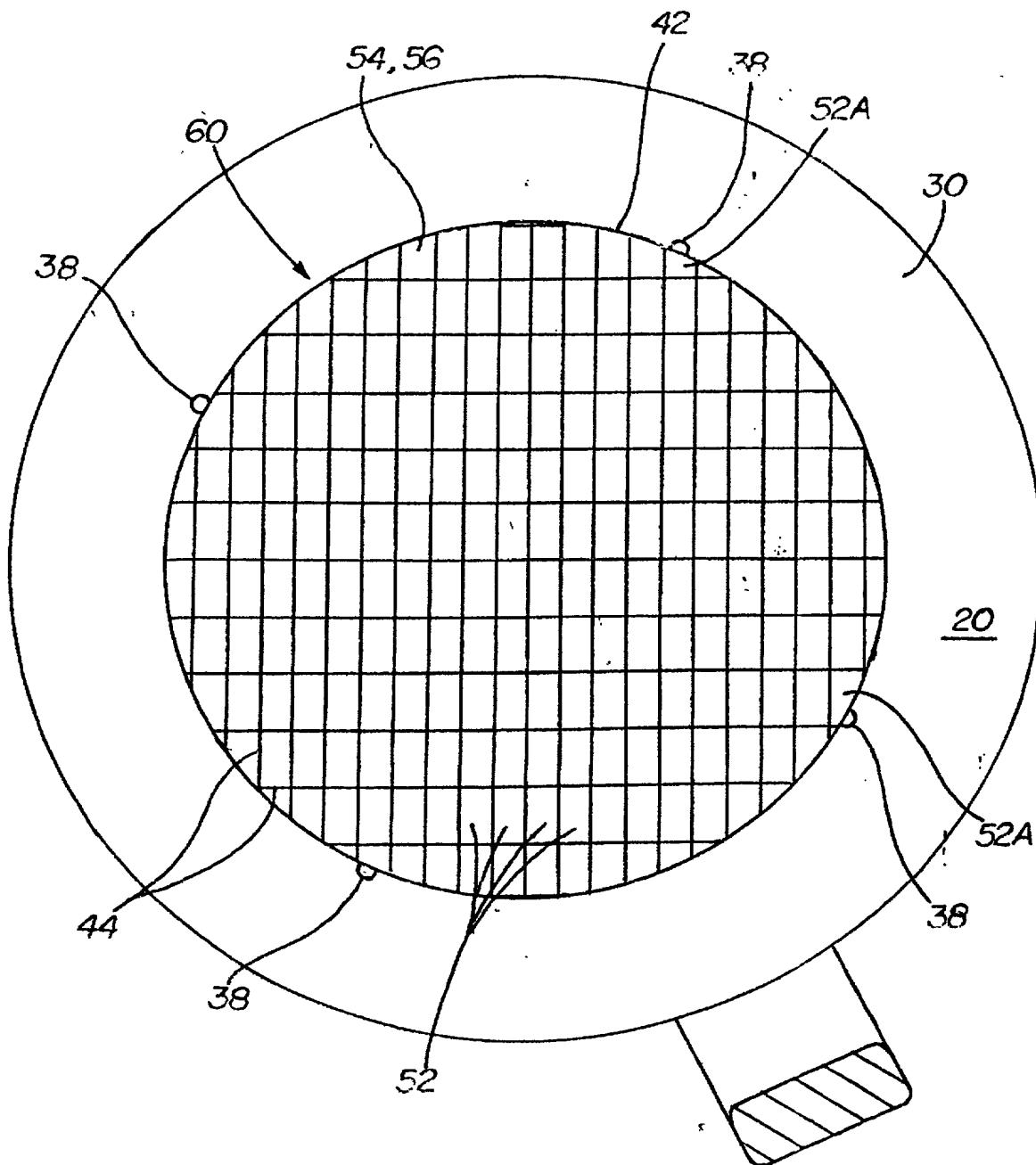


FIG. 2

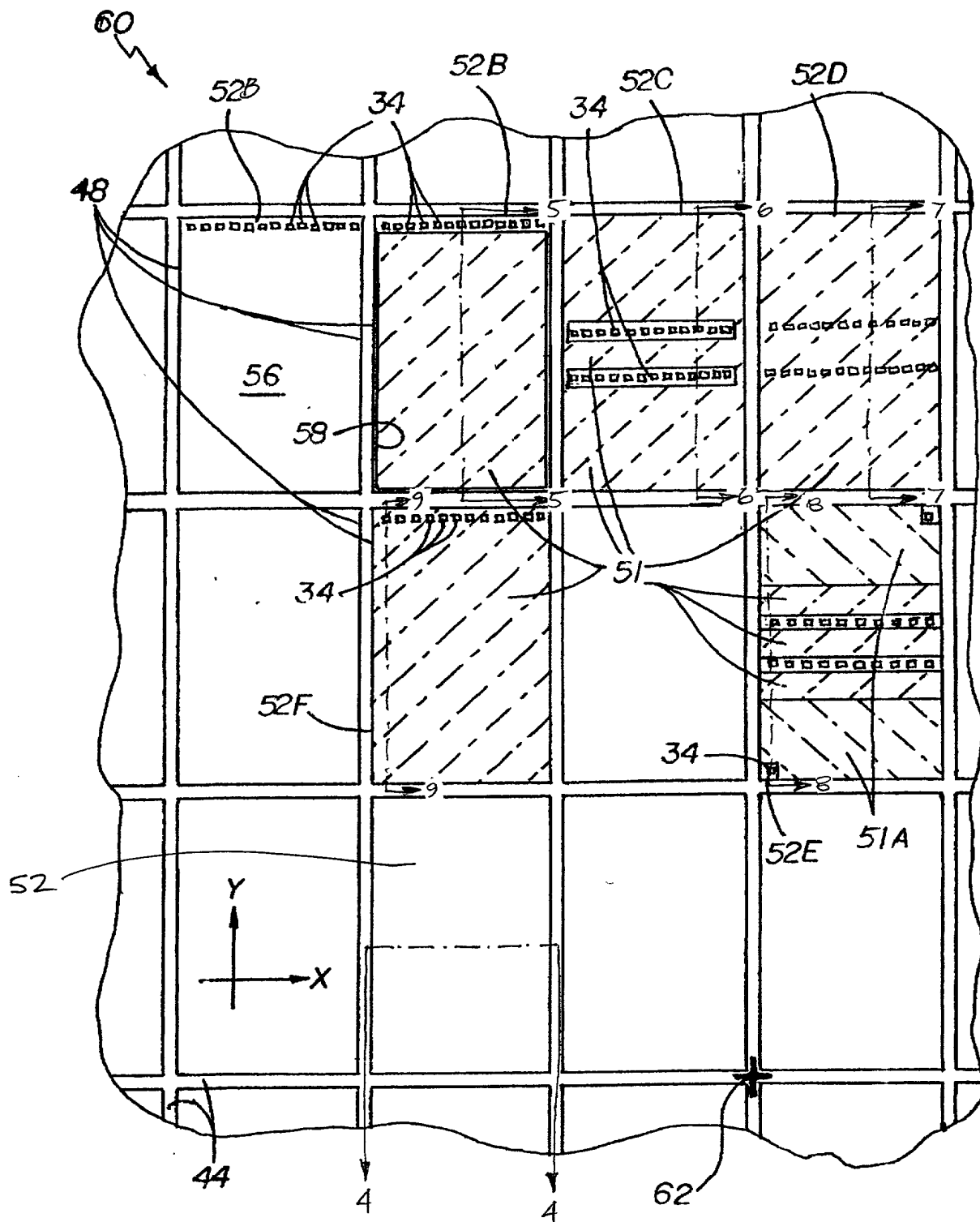


FIG. 3

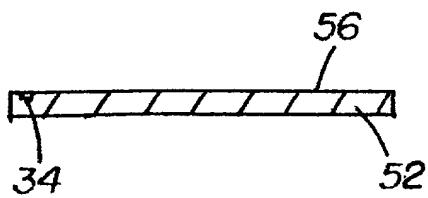


FIG. 4

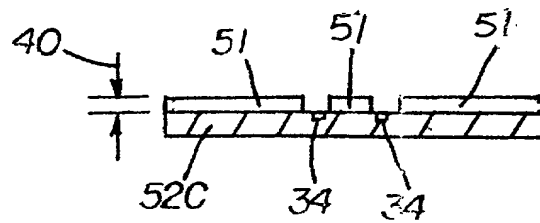


FIG. 6

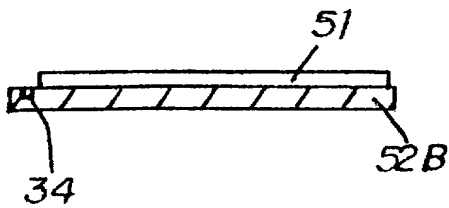


FIG. 5

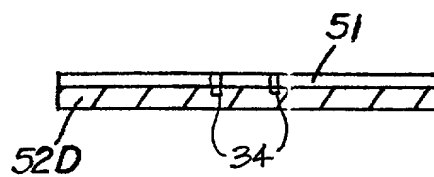


FIG. 7

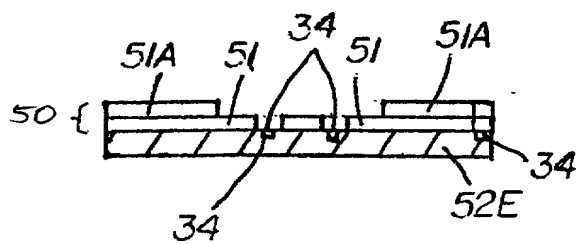


FIG. 8

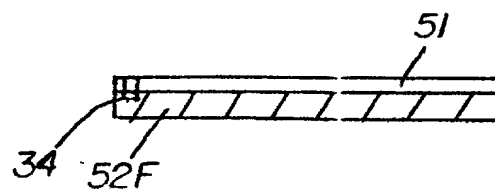


FIG. 9

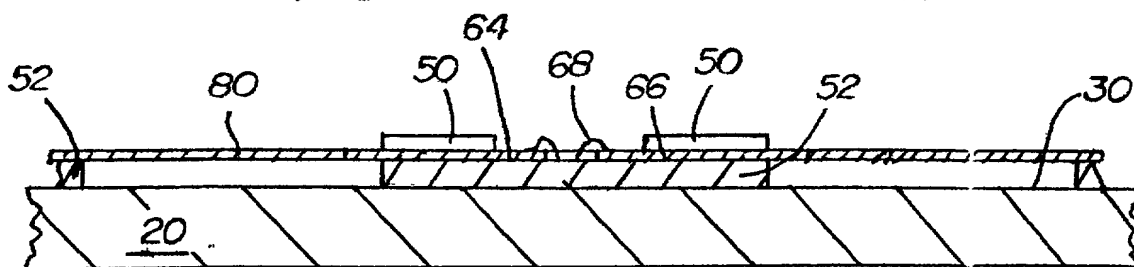


FIG. 10

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled STEREOLITHOGRAPHIC METHODS FOR FORMING A PROTECTIVE LAYER ON A SEMICONDUCTOR DEVICE SUBSTRATE AND SUBSTRATES INCLUDING PROTECTIVE LAYERS SO FORMED, the specification of which (check one):

☒ is attached hereto.

☐ was filed on _____ as United States application serial no. _____ and was amended on _____.

☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

Priority Claimed

(number)	(country)	(day/month/year filed)	Yes	No
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
_____	_____	_____
_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)
_____	_____

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012
 Laurence B. Bond, Reg. No. 30,549
 Allen C. Turner, Reg. No. 33,041
 Stephen R. Christian, Reg. No. 32,687
 Paul C. Oestreich, Reg. No. 44,983
 Kenneth C. Booth, Reg. No. 42,342
 Kerry D. Tweet, Reg. No. P-45,959

William S. Britt, Reg. No. 20,969
 Joseph A. Walkowski, Reg. No. 28,765
 Kent S. Burningham, Reg. No. 30,453
 Brick G. Power, Reg. No. 38,581
 Devin R. Jensen, Reg. No. 44,805
 Samuel E. Webb, Reg. No. 44,394
 Michael L. Lynch, Reg. No. 30,871

Thomas J. Rossa, Reg. No. 26,799
 James R. Duzan, Reg. No. 28,393
 Edgar R. Cataxinos, Reg. No. 39,931
 Kenneth B. Ludwig, Reg. No. 42,814
 Eleanor V. Goodall, Reg. No. 35,162
 David L. Stott, Reg. No. 43,937
 Lia M. Pappas, Reg. No. 34,095

Address all correspondence to:

Brick G. Power, telephone no. (801) 532-1922.
TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: Warren M. Farnworth

Inventor's signature: Warren M. Farnworth

Residence: Nampa, Idaho

Citizenship: U.S.A.

Post Office Address: 2004 S. Banner, Nampa, ID 83686-7271

Date: 02-28-2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Warren M. Farnworth et al.
 Serial No.: Not yet assigned
 Filed:
 Title: STEREO LITHOGRAPHIC METHODS FOR FORMING A PROTECTIVE LAYER ON A SEMICONDUCTOR DEVICE
 SUBSTRATE AND SUBSTRATES INCLUDING PROTECTIVE LAYERS SO FORMED

Examiner: Unknown
 Group Art Unit: Unknown
 Attorney Docket No.: 3923US (99-0033)

**POWER OF ATTORNEY BY ASSIGNEE
 AND CERTIFICATE UNDER 37 CFR § 3.73(b)**

Assistant Commissioner for Patents
 Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Edgar R. Cataxinos, Reg. No. 39,931
Stephen R. Christian, Reg. No. 32,687	Brick G. Power, Reg. No. 38,581	Kenneth B. Ludwig, Reg. No. 42,814
Paul C. Oestreich, Reg. No. 44,983	Devin R. Jensen, Reg. No. 44,805	David L. Stott, Reg. No. 43,937
Kenneth C. Booth, Reg. No. 42,342	Samuel E. Webb, Reg. No. 44,394	Kerry D. Tweet, Reg. No. P-45,959
Eleanor V. Goodall, Reg. No. 35,162	Michael L. Lynch, Reg. No. 30,871	Lia M. Pappas, Reg. No. 34,095

as its attorneys with full power of substitution to prosecute this application and all applications claiming filing date priority therefrom and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

- ☐ In an assignment recorded in the U.S. Patent and Trademark Office at Reel , Frame .
☒ In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

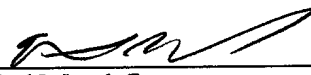
Please direct all communications regarding the above-identified application to:

Brick G. Power,
 TRASK, BRITT & ROSSA
 P.O. Box 2550
 Salt Lake City, UT 84110
 Tele: (801) 532-1922
 Fax: (801) 531-9168

Respectfully Submitted,

MICRON TECHNOLOGY, INC.

Date: 3-2-01

By: 
 Michael L. Lynch, Esq.
 Reg. No. 30,871
 Chief Patent Counsel,
 MICRON TECHNOLOGY, INC.

PATENT

Attorney Docket No. 3923US (99-0033)

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, each undersigned ASSIGNOR does hereby:

SELL, ASSIGN AND TRANSFER to MICRON TECHNOLOGY, INC. ("ASSIGNEE"), a corporation of the state of Delaware having a place of business at 8000 South Federal Way, Boise, ID 83707-0006, the entire right, title and interest for the United States and all foreign countries in and to any and all improvements which are disclosed in the Application for United States Letters Patent, which has been executed by each undersigned ASSIGNOR concurrently herewith and is entitled STEREOGRAPHIC METHODS FOR FORMING A PROTECTIVE LAYER ON A SEMICONDUCTOR DEVICE SUBSTRATE AND SUBSTRATES INCLUDING PROTECTIVE LAYERS SO FORMED, such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent or the legal equivalent thereof which have been or may be filed in the United States and all foreign countries relating to any of such improvements; all original, reexamined and reissued patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such application made in the United States;

AUTHORIZE the ASSIGNEE to apply for and receive any and all United States and foreign patents relating to such improvements in its own name;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to and in the name of the ASSIGNEE;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement or encumbrance affecting the rights and property herein conveyed has been or will be made or entered into by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

COVENANT, when requested and at the expense of the ASSIGNEE, to carry out in good faith the intent and purpose of this assignment, to execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications relating to any and all such improvements; to execute all rightful oaths, declarations, assignments, powers of attorney and other papers; to communicate to the ASSIGNEE all facts and provide to the ASSIGNEE all documents and things known and accessible to the undersigned relating to such improvements and the history thereof, and testify as to the same in any interference, litigation or other proceeding relating thereto; and generally to do everything possible which the ASSIGNEE

shall consider desirable for vesting title to such improvements in the ASSIGNEE, and to secure, maintain, defend and enforce valid and enforceable patent protection for such improvements;

AGREE AND ACKNOWLEDGE that the SALE, ASSIGNMENT AND TRANSFER of rights and property set forth herein is and shall be IRREVOCABLE and BINDING upon the heirs, assigns, representatives and successors of each undersigned ASSIGNOR and EXTEND to the successors, assigns and nominees of the ASSIGNEE.

ASSIGNORS:

Warren M. Farnworth
Warren M. Farnworth

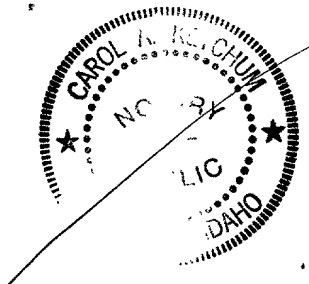
Date 2-28-2000

Alan G. Wood
Alan G. Wood

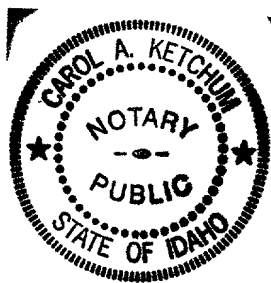
Date 2/28/00

STATE OF _____)
: ss.
COUNTY OF _____)

BEFORE ME, the undersigned authority, on this 28th day of February, 2000, personally appeared Warren M. Farnworth, personally known or proven by satisfactory documentary evidence to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he executed the same of his own free will for the purposes and consideration therein expressed.

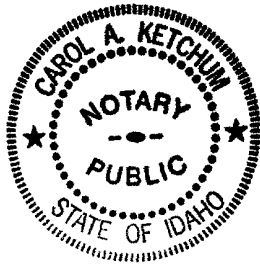


Carol A. Ketchum
Notary or Consular Officer



STATE OF _____)
 : ss.
COUNTY OF _____)

BEFORE ME, the undersigned authority, on this 28th day of February, 2000,
personally appeared Alan G. Wood, personally known or proven by satisfactory documentary
evidence to me to be the person whose name is subscribed to the foregoing instrument and
acknowledged to me that he executed the same of his own free will for the purposes and
consideration therein expressed.



Carol A. Ketchum
Notary or Consular Officer

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